

Trends in Digital Imaging

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ABSTRACT

High dynamic range CMOS (HDRC[®]) imager technology, which is a special digital imaging concept suitable for a wide variety of applications, is reviewed in this paper. Important aspects of pixel cell layout and circuit/system design, based on which this CMOS imager concept is fully exploited, are discussed. Various applications of HDRC[®] are illustrated and future directions are indicated.

1. INTRODUCTION

Integrating image sensing devices, such as those based on the well known charge-coupled devices (CCDs), accumulate the photon generated electrons or holes in the surface field generated potential wells of deep depleted MIS diodes. Dynamic range and signal-to-noise (S/N) ratio of a single collected image are strongly correlated with shot noise and the so called readout noise of charge transfer and output amplification. Common CCDs offer a single shot dynamic range of 50 dB to 80 dB, depending on the particular application (i.e. video or still image capturing) [1]. Well known strategies for extending the dynamic range are a sequence of readouts at different integration times, time-to-saturation, well-capacity adjusting and self-reset [2],[3]. Most of the integrating CMOS imagers use diffused photodiodes in combination with in-pixel amplification [4]. Their blooming resistant photodiodes and the non-destructive readout allow a number of individually timed readouts within the same integration period. For dynamic range extension this readout is typically combined with a piecewise linear compressed output signal.

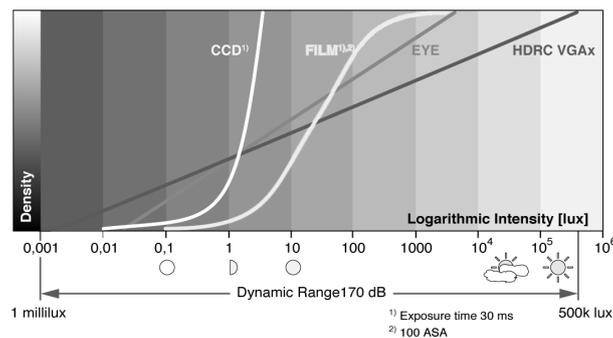


Fig. 1: Dynamic range of different image sensors.

In contrast, the patented HDRC[®] (High Dynamic Range CMOS) circuit uses the exponential sub-threshold characteristics of a MOS transistor [5],[6]. This transistor is directly connected to the photodiode as a permanent working shunt for photocurrents extending over more than 8 orders of magnitude. This results in a logarithmic current to voltage conversion with unsurpassed single shot dynamic range of 170 dB (Fig. 1).

2. HIGH DYNAMIC RANGE IMAGING

For many years the different potential pixel designs of CMOS imager pixel cells have been investigated and compared. Today's favourite structure for HDRC[®] is based on a n^+p junction in a low doped p-substrate. This arrangement provides an optimum combination of low photodiode leakage current and spectral response.

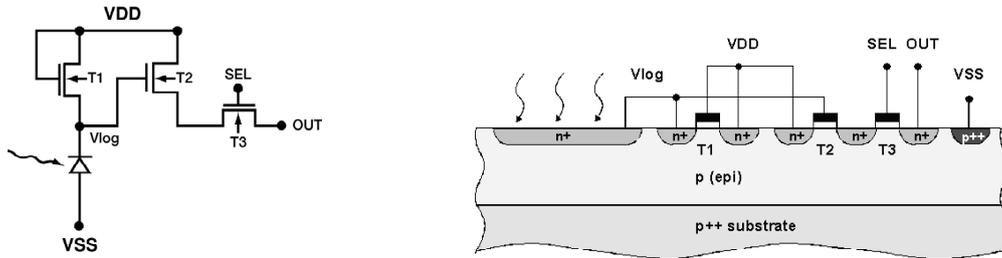


Fig. 2: HDRC[®] logarithmic compressing pixel.

In Fig. 2, as an example, the generic circuit consisting of a photodiode, a logarithmic compression transistor (T1) and additional buffer transistors T2 and T3 are depicted. The logarithmic transistor T1 is connected to the high bias potential V_{DD} , while the photodiode is at low bias V_{SS} . Note, that historically the complimentary sensor implementation, i.e. a p^+n photodiode in a n-well, has been used. The logarithmic HDRC[®] principle is based on a continuous current-to-voltage conversion by a transistor operating in the sub-threshold regime. It is evident that the dynamic range is directly related to the range and accuracy of the sub-threshold regime of the MOS transistor.

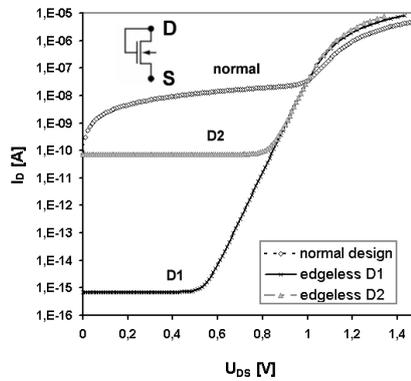


Fig. 3: Measured sub-threshold characteristics of different MOS transistor layouts.

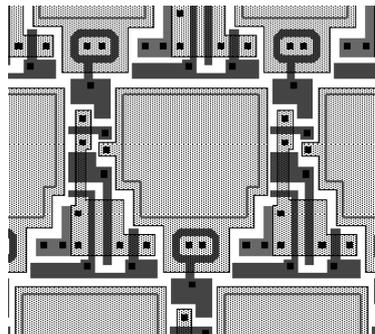


Fig. 4: HDRC pixel array layout.

While shallow trench isolation (STI) is the state-of-the-art device isolation structure, it is not the optimum technology for HDRC[®] image sensor implementations in CMOS, since it is prone to the formation of a parasitic edge transistor [7]. The leakage current level of such a transistor is therefore unacceptably high (“normal design” in Fig. 3). A solution is derived from a so-called edgeless transistor layout with two possible implementations, depending if the source (“D1” in Fig. 3) or the drain (“D2” in Fig. 3) is defined as the inner contact of the structure. Note, that only the configuration D1 shows the required sub-threshold range of 8 orders of magnitude. For illustration purposes the layout of a HDRC[®] pixel cell is shown in Fig. 4 [7]. The large feature in the centre serves as the photosensitive element. The edgeless transistor is located at the lower side, working in logarithmic mode. Also visible is the amplifier circuitry provided with each pixel.

3. CMOS IMAGER SYSTEM

The CMOS image sensor as the heart of an imager system on the one hand defines the optical properties of the imager system, such as sensitivity, spectral response and dynamic range. On the other hand its layout and design determines the resolution, readout speed, random access of regions of the viewed scene and the kind of sampling in time of the image information, which are all related to the circuit design. Basically there are two different sampling mechanisms, i.e. line synchronous and frame synchronous sampling [8],[9], also described as rolling shutter and global shutter. Fig. 5 shows a high dynamic range scene with a light bulb and a rotating fan at 3000 rounds per minute (rpm) captured with a rolling and a global shutter HDRC[®] sensor. In comparison, the rolling shutter leads to geometric distortions at objects moving at high speed whereas with the global shutter the wings of the fan were captured in their original shape with sharp edges.



Fig. 5: Image distortion with high speed moving objects: HDRC sensor with rolling shutter readout (left image) and with a global shutter (right image).

In this paper we present the combination of the HDRC[®] principle for high dynamic range imaging with a sampling element in each pixel. Fig. 6 shows the HDRC[®] global shutter pixel cell with the photodiode, the logarithmic compressing transistor operating in the sub-threshold regime, a hold capacitor and a shutter transistor that is controlled by an on-chip timing generator. The pixel has a pitch of 10 μm , a fill factor of $\sim 25\%$ and a low light sensitivity of 4 mLux. A sensor with a resolution of 768x496 pixels at 30 frames per second and a dynamic range of 130 dB has successfully been realized. Random accesses of regions of interest at higher frame rates are programmable by a serial interface, e.g. 140x70 pixels at 1200 frames per second.

As a consequence of the logarithmic photocurrent to voltage conversion by the log transistor operating in the sub-threshold region, the sensor exhibits a pixel to pixel offset variation mainly caused by the transistor’s threshold voltage distribution, also known as fixed-pattern noise. This fixed-pattern noise is corrected in the camera or imaging system after analog to digital conversion by subtracting the offset values of each pixel according to offset values stored e.g. in a flash memory of 512k x 8 bit. Fig. 7 shows a simplified block diagram of the signal path from the pixel to the ADC and the controller performing the fixed-pattern correction.

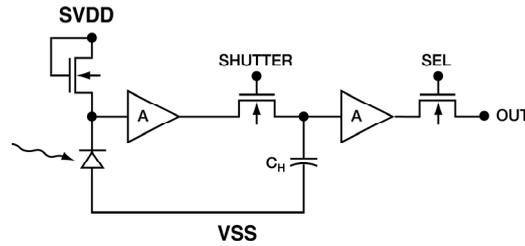


Fig. 6: HDRC® pixel cell with global shutter

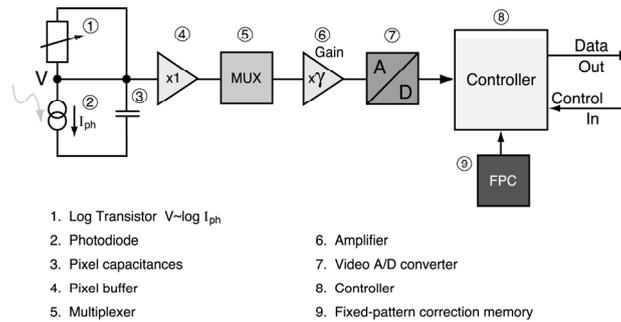


Fig. 7: Signal path from the pixel to the digital output data of a HDRC® camera or imaging system.

4. APPLICATIONS

Applications of the HDRC® sensors with rolling or global shutter and high demands on the dynamic range and the readout speed of the sensors are in machine vision e.g. metal surface inspection [10], automation or welding seam inspection with laser triangulation. Fig. 8 shows a typical scene captured with a HDRC® sensor developed for a night vision driver assistance system. In this automotive application the challenges for the sensor are the wide spectral sensitivity from visible (VIS) to near infrared (NIR), to recognize the lane and obstacles far away on the dark road without getting blinded by the high beam of the approaching car [11],[12].

Also advanced systems in traffic control, security and surveillance need robust image acquisition in tough lighting conditions with high scene contrasts in the low as well as in the bright parts. The logarithmic conversion function of the HDRC® sensor enables a 2% contrast resolution over 6 decades of illumination. An example of such kind of image processing is the HDRC®-based camera guided aircraft docking system [13]. This system is installed on several international airports worldwide [14],[15] (Fig. 9).



Fig. 8: Night scene illuminated with (NIR) high beam.



Fig. 9: Camera guided aircraft docking system using a HDRC® camera (courtesy: GEVITEC).

Furthermore, in the field of medical applications there is a growing market for image sensors integrated in endoscopes or inspection instruments for minimal-invasive surgery. The miniaturization of the sensor and the optimization of the image quality are the major challenges. The sensor shown in Fig. 10 has a $4.6 \mu\text{m}$ HDRC® pixel with a logarithmic characteristic, a resolution of 180×200 pixels and a small number of I/O ports. With this approach a chip size of $1.3 \times 1.7 \text{ mm}^2$ was realized [16]. The assembled endoscope tip ($\varnothing 3.5 \text{ mm}$) is one of the smallest CMOS video probes to date.

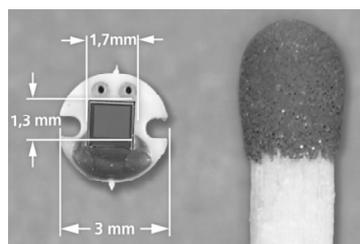


Fig. 10: Miniaturized HDRC® sensor for endoscopy mounted on a ceramic plate in comparison to a match.

5. NEW DIRECTIONS

Patterning HDRC® sensors with Bayer mosaic color filters result due to the logarithmic response in an illumination-independent color constancy of the images. A color enhancement algorithm is used giving photographic film like images with good color saturation.

Performance improvements of the photo-sensing element are a major task in future image sensor development. The Thin-Film-on-CMOS (TFC) technology is one approach to address this issue. It uses the low temperature deposition of amorphous silicon photodiodes on top of CMOS image sensors for the fabrication of p-i-n layer diodes [17], [18]. These TFC diodes have a fill factor $> 90\%$ and a low dark current. Characteristics such as the spectral response can be adapted to the application independently of the CMOS process, i.e. effectively as an add-on process. First results obtained with a TFC image sensor demonstrate sharp and high contrast images (Fig. 11).



Fig. 11: TFC sensor Image of a landscape scene.

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